

Simple, Wide Tuning Range 1-5 Ghz VCO With High PSRR

Kevin Aylward B.Sc. AnaSoft Ltd.

Abstract - This paper describes a high-speed voltage controlled oscillator, which has both a wide tuning range and high power supply rejection ratio. The design presented here is simulation based and utilizes the tmsc 0.18u cmos process. Typical applications of the VCO are for components in high speed, low jitter phase locked loops.

Index terms - voltage controlled oscillator, phase locked loop.

1. Introduction

The design of low noise, high speed, wide range voltage controlled oscillators are particular problematic because of their conflicting requirements. Specifically, the ability to sweep the oscillator frequency over a wide range, and the ability to minimize noise. It is usually the case that a wide sweep range implies that noise will have a corresponding larger effect on frequency variations. For example, an LC tuned oscillator will reduce noise significantly if it has a high Q. However, high Q circuits are difficult to tune over a wide range.

2. Design Goal

The design goal of this paper is the design of vcos to be used in a mixed-mode, low jitter phase locked loop systems. This type of system is typically subjected to significant amounts of digital noise, in addition to the issues resulting from process variations. The approach taken therefore, is one to minimize the effect of power supply noise, yet with a circuit topology that still allows for a wide tuning range. In addition, the design should be *simple*.

3. Prior techniques

Typical techniques to solve these design goals are often complex. For example, to minimize the effect of noise, a narrow tuning range might be used, i.e. a vco with a low F/V gain constant. This then might require a bank of such oscillators, all with a different nominal center frequency with extensive logic to select the vco with the desired center frequency. This is because process variations are often too large to guarantee that one vco will have a center frequency of sufficient accuracy.

4. Methodology

The design approach taken here is one of engineering simplicity. All too often complicated designs are undertaken that, on closer examination, do not actually achieve any net benefit then simpler designs. The design presented here, might even be said to be rather pedestrian when compared to some others that appear in the literature. However, such simplicity is usually a bonus. It allows for a much easier analysis of operation and subsequently more confidence that the design will be robust in the field.

5. Principles

5.1 Noise considerations can imply differential approaches.

In general, differential circuits have much better noise interference rejection than signal ended circuits. This leads to the conclusion that the main vco amplifiers should be fully differential based.

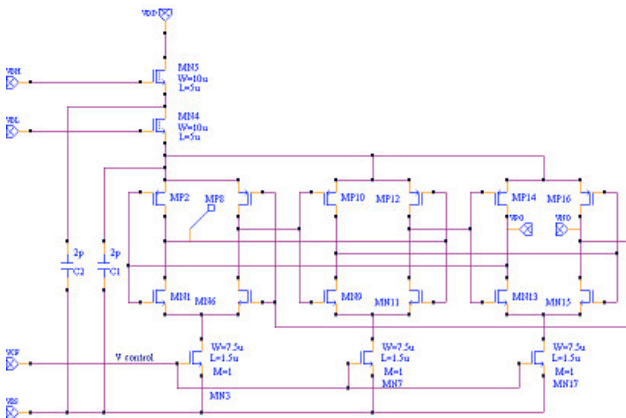
5.2 Wide tuning range can imply a single ended control in low voltage applications.

To achieve a wide frequency control range, currents must be swept over a large range. In a conventional differential amplifier this is difficult to achieve due to a fixed bias current. Class AB differential stages are better, but are difficult to construct when the supply voltage is limited. This led to the conclusion of controlling a current using a single mosfet. This allows a current variation from essentially zero to the maximum allowed at a gate voltage equal to the supply voltage.

6. Design Details

6.1 Its hard to beat a simple cmos nmos/pmos inverter for gain bandwidth product.

Many amplifier topologies were examined. The simplest differential one was chosen.



This is a standard 3 stage differential amplifier with pmos loads, connected in an oscillating ring loop. A vco control voltage controls the tail currents of each of the stages, which changes the delay/phase response of the loop, and thereby the frequency. Supply rejection is achieved by the use of two source follower connected natural nmos devices.

The novelties of this design are the direct filtering of the supply by *small* nmos devices *right* at the vco, and the control of the operating current with an nmos device reference to *ground*. These small power supply filtering devices minimizes capacitive feedthrough from the supply, and the ground referenced control current also minimizes supply coupling.

7. Operating Conditions

Transistor sizes of the oscillator were set to their minimum valuses, i.e. $W=0.22\mu$, $L=0.18\mu$.

Nominal supply voltage was 3.3 volts, but with the vco transistors biased such that their voltage did not exceed 1.8V, which is the limit for these tmsc devices.

At a V control of 0.5V, frequency was 1.9Ghz at 18ua supply current.

8. Basic Results

At a V control of 0.6V Nominal supply current is 55ua at an oscillation frequency of 4.6Ghz.

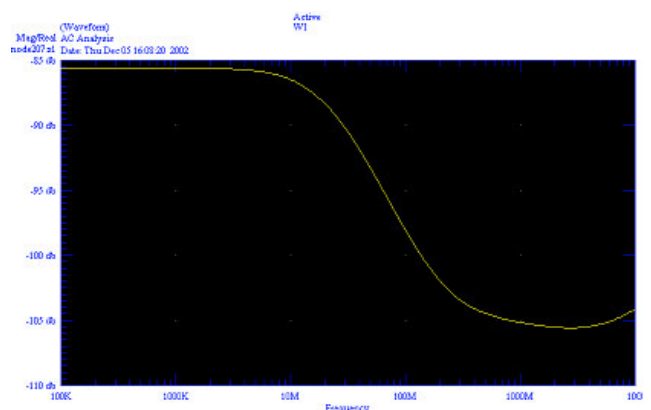
At a V control of 1.0V, frequency was 5.2Ghz at 65ua supply current.

With ideal bias voltages, PSRR was better than 80db from DC to 10Ghz.

The bias voltages for the PS filtering devices are crucial, and in practice derived from another special, high rejection ratio bias generator. Such a bias circuit is described in another paper by the author.

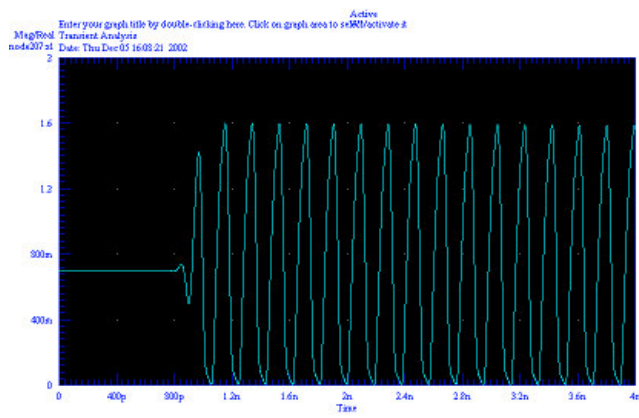
9. Simulation Graphs

Power supply rejection ratio



Channel length was the main determinat of supply rejection at low frequencies, achieving 85db rejection with $L=5\mu$ at DC. The 2 of 2pf capacitors ensure 100db rejections above 100Mhz,

Transient response



10. Conclusions

A very *simple*, wide tuning range, high supply rejection ratio, voltage controlled oscillator was described.