
Flicker Noise Nullification In Oscillators

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Overview

It is demonstrated that $1/f$ flicker noise in oscillators can, in principal, be completely eliminated by a technique of Flicker Noise Nullification. That is, an effect where low frequency device additive noise becomes up-converted to phase noise around the oscillator frequency. However, it is conclusively demonstrated that a conventional explanation as to how this type of nullification might occur is false.

This nullification is attributed to the construction of a zero value for the integral of the “ISF” of the HL-LTV theory, despite the waveforms being not symmetrical and the fact that it is proved in [LTV](#) that the HL-LTV theory is incorrect. Indeed, it is arguably, because the real inherent non-linearity of any possible ISFs has not been understood, that such a nullification technique has similarly not been forthcoming to date.

Introduction

In “The Designers Guide To High Purity Oscillators” (DGO) by Emad Hegazi, Jacob Rael and Asad Abid, it was put forward an explanation and technique for the elimination of up-converted $1/f$ noise. The actual explanation possibly being rather obtuse for many analog designers, with unfamiliar terms and almost “Star Trek” speak according to this author.

The thrust of the argument was that ... there is no path for the low-frequency noise to a common mode capacitance...“...flicker noise is stored on the floating capacitor...”.

The circuit is a differential amplifier, connected as an oscillator, with the emitters coupled with a capacitor. Conventional wisdom would have described the amplifier as having additional emitter negative feedback impedance to lower the gain for low frequencies but keep the gain up for high frequencies. Unfortunately, although this explanation works for small signal analysis, and does indeed reduce the output noise for a normal differential amplifier, both variants of these, arguably, equivalent explanations, turn out to be incorrect. Simulations show quite clearly that the phase noise of the circuit is as if it has the same open loop baseband noise, over all frequencies, irrespective of any value of capacitor. That is, *the capacitor makes absolutely no difference to the ability to null out all $1/f$ noise.*

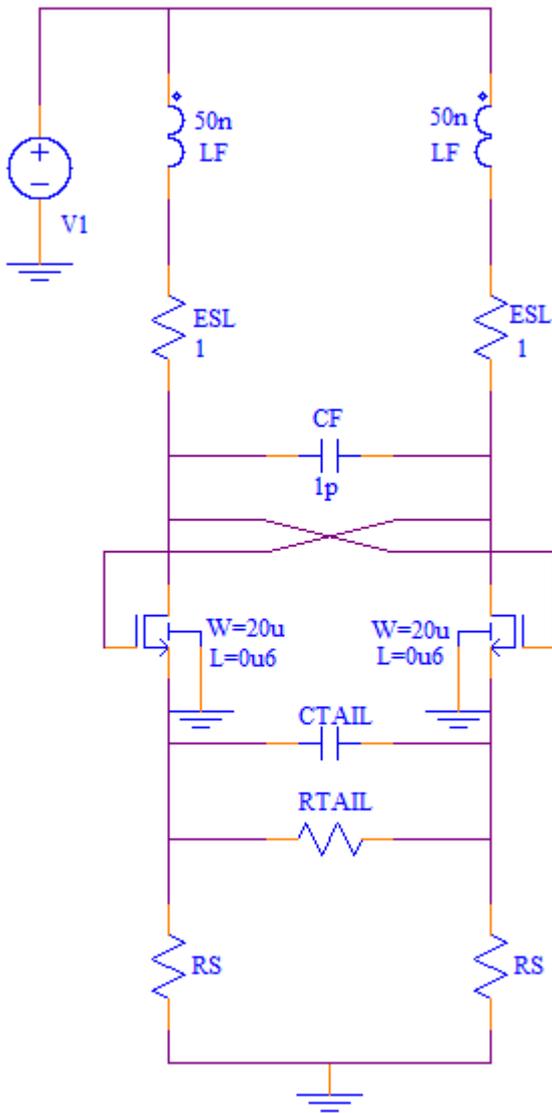
The same authors in their paper, “A 1.5V, 1.7mA 700 MHz CMOS LC Oscillator with No Upconverted Flicker Noise” also allude to a technique to completely eliminate $1/f$ noise. However, on examination, and as noted in that paper, only reduces $1/f$ noise down to 2kHz offsets. It is clear from their graphs that $1/f$ is still present, and that arguably, it is only the additional noise of the additional current source that has been eliminated by their technique.

It is shown here, that the discussed elimination of $1/f$ noise, has a 20db/dec slope right down to 1 Hz offset from a 10 MHz offset.

Description

The equivalent topological schematic of the nulling circuit is shown here:

Fig. 1



Where for the DGO version there is no RTAIL resistor, and with no specified values to the components. The values specified here are the ones used in the simulations discussed here. The devices being NMOS from the XFAB XBO6 0.6u BiCMOS process.

Cadence SpectreRF standard phase noise analysis was used for all results. Accuracy was set to 1e-6 with the number of harmonics set to 50.

The oscillator's nominal frequency was 500 MHz. Values of RS and CTAIL were adjusted. Principally, RTAIL was set to 1G ohm or 10 mohm to alternate introduce or eliminate CTAIL. Checks were also performed at different widths and lengths of the Mosfets.

It was clearly determined that irrespective of the value CTAIL, that a nullification adjustment could be made of RS that resulted in complete elimination of 1/f up-converted noise. This was ascertained by noting that the noise profile produced a clean 20db/dec slope rather than a 30db/dec slope usually for the presence of 1/f noise.

Tuning of the null point was quite sensitive, of the order of one ohm or so. Results were taken for a semi null point above and below, where the noise corner was still significantly reduced in addition to the true null point. For the semi null point, CTAIL made, essentially, no difference whatsoever to the null point.

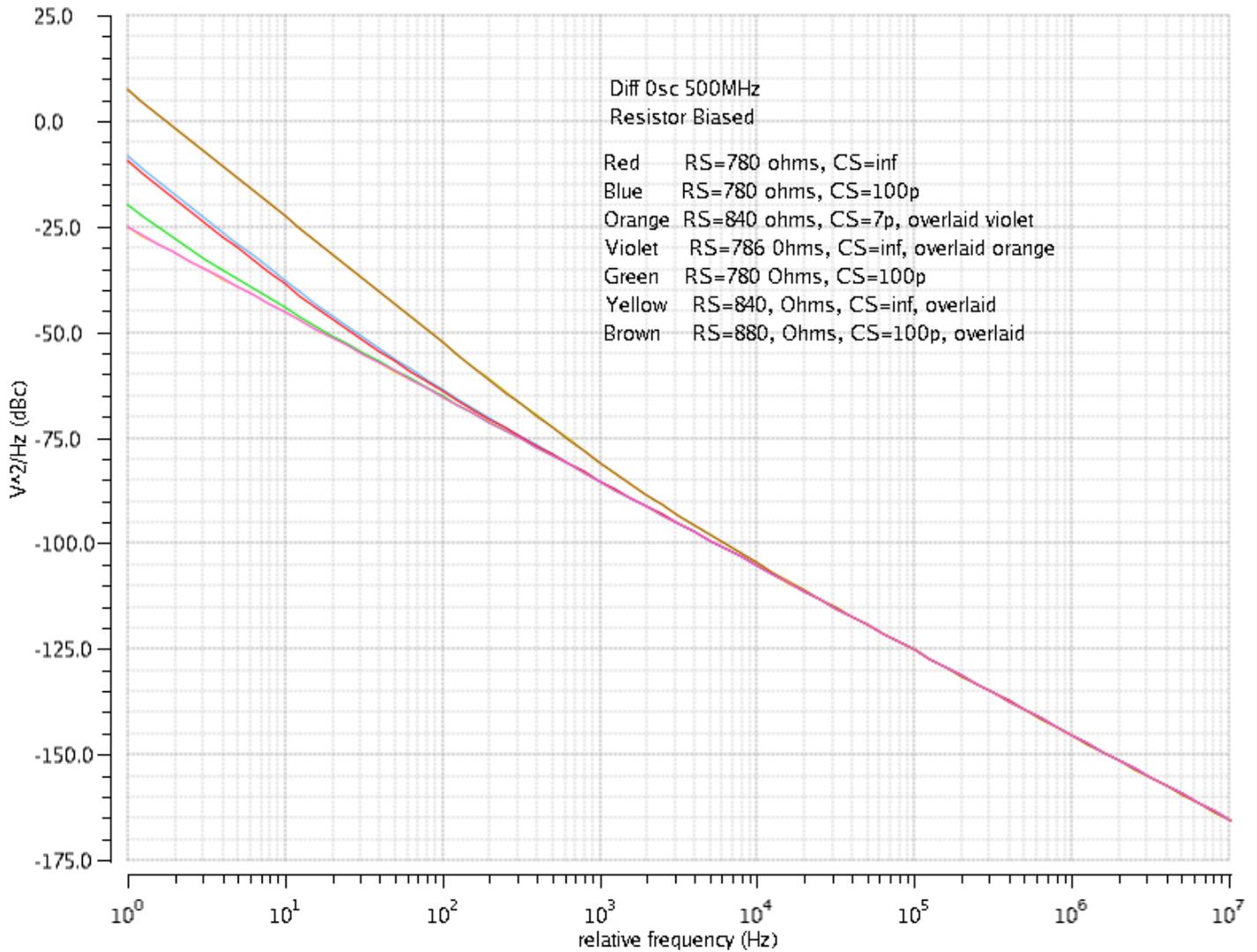
In an effort to determine why there may have been a misunderstanding that CTAIL was required to be tuned, RS was set to a semi tuned value and CTAIL was varied. It was determined that there was then a specific value

for CTAIL that re-introduced the full resistive valued null. However, this optimum varied CTAIL value only produced a graph that overlaid the optimum resistive tuned graph.

Results

Fig. 2

Resistive Tuning of 1/f Null



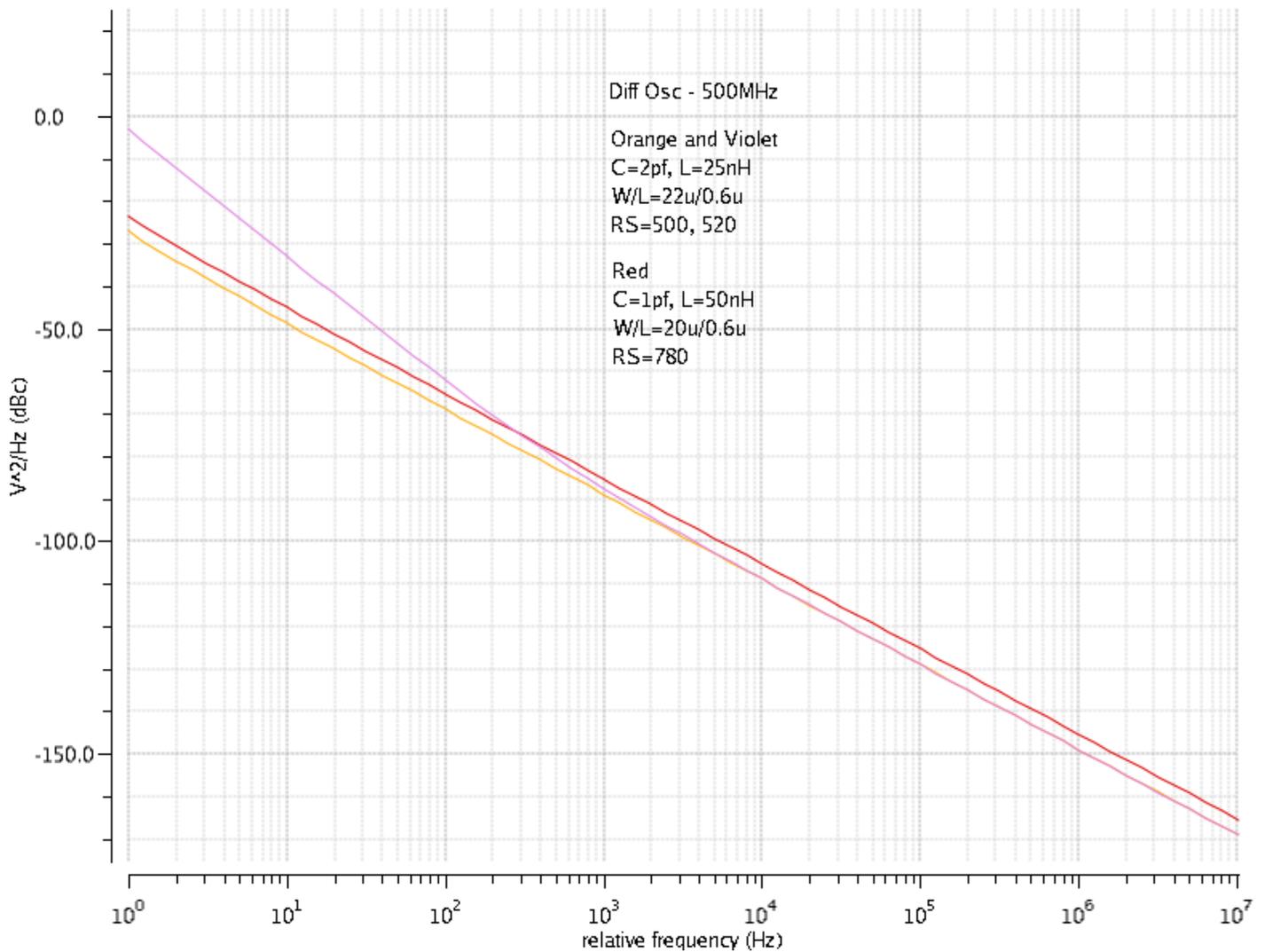
This graph shows the following:

- 1 No value of capacitance nulling produced noise less than that produced by resistive tuning.
- 2 Red and Blue show no difference between 100p and shorted capacitor at semi null
- 3 Orange tuned 7p cap with semi nulled resistive forming full null, overlaid resistive tuning null
- 4 Noise is completely independent of the expected changes in small signal value.

To check that the circuit was not a one off pathological ability to null 1/f noise via resistive tuning, simulations were also run with the inductor halved to 25nH and the capacitor doubled to 2pf.

Fig. 3

Alternate Tank Values



For the alternate tank values, the widths were determined to be slightly different, now becoming 22u compared to 20u, with the nulling point resistor now reduced to 500 ohms.

Red - original tank value nulled phase noise

Orange – alternate tank values at nulled pint

Violet – alternate tank values, 20 ohms off null.

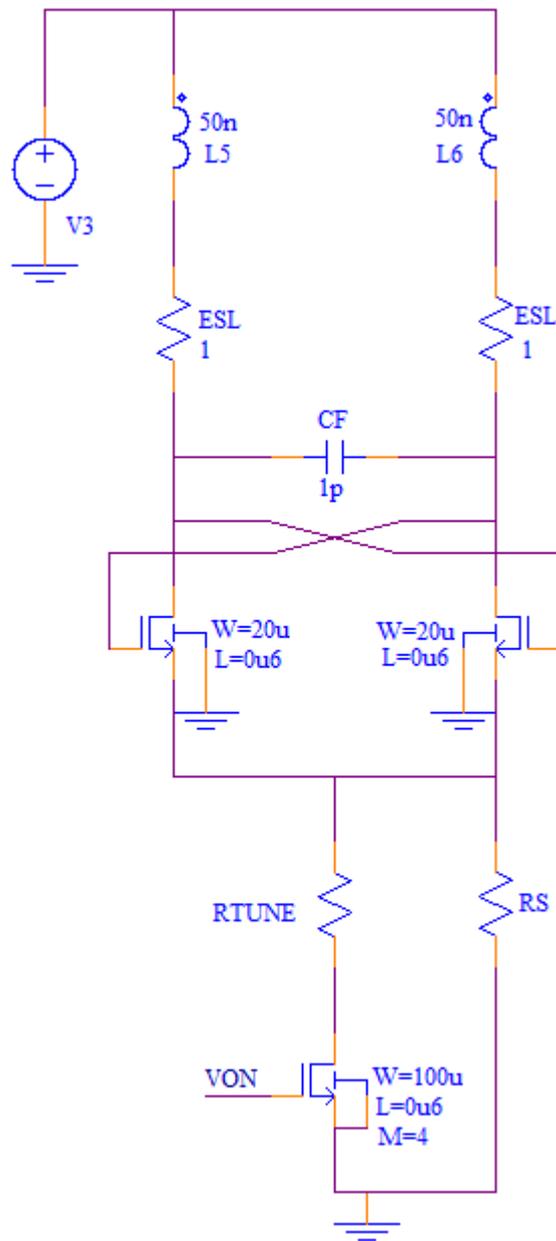
Nullability

The null point is quite sensitive, therefore for this to be of any value in a real product simulations were performed to determine whether the null point could be reliably digital tuned with mosfet switches. The issue here being whether or not adding in mosfet switches would add noise due to their own 1/f noise.

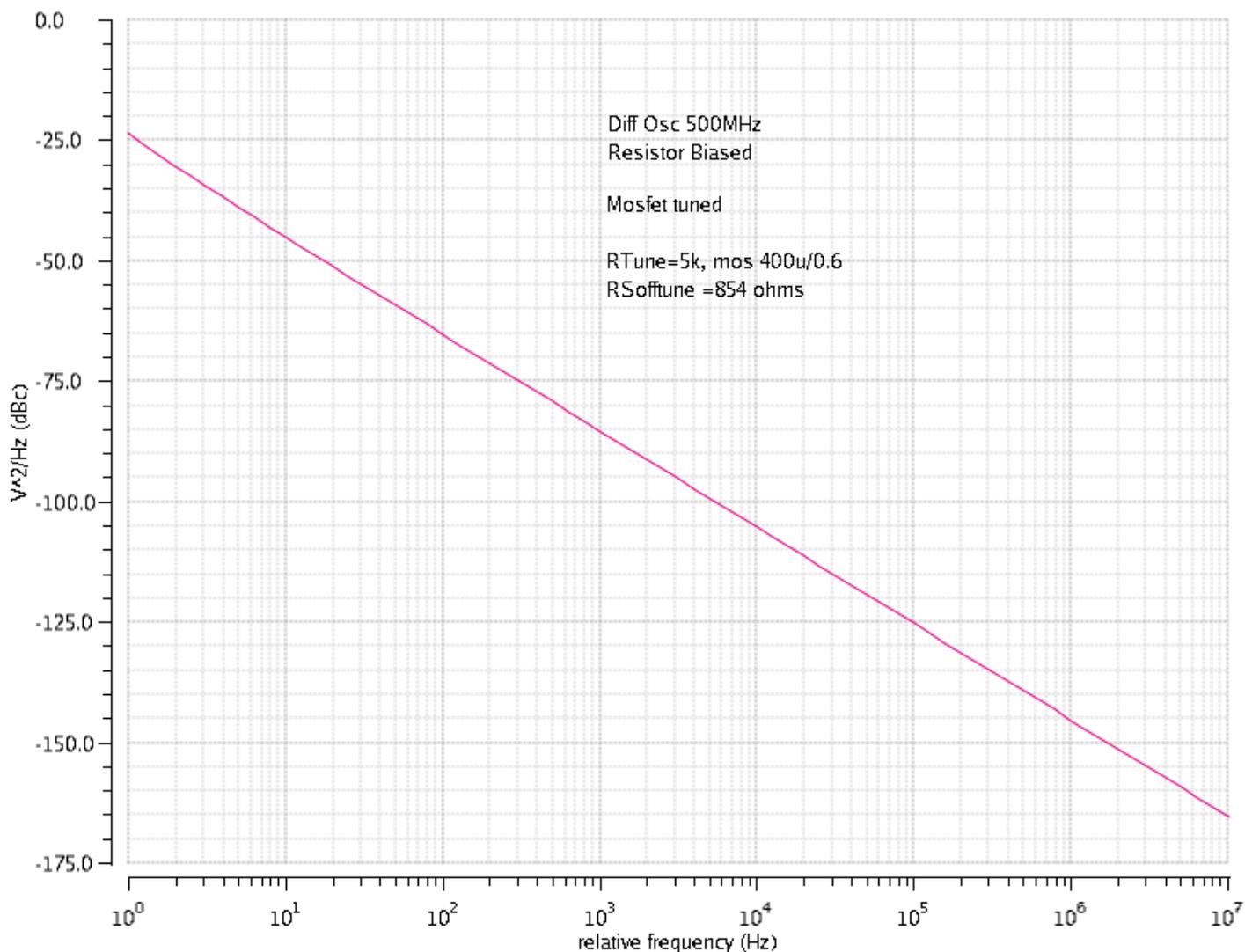
RS was increased to mimic a non nulled process variation, and nulled with another resister, switched via a mosfet.

Fig. 4

Digital Tunability Schematic



Digital Tunability Phase Noise



The graph shows that a conventional digital mosfet switch arrangement may be used to bring an untuned circuit back on tune without adding any additional 1/f noise. It is thus viable to use standard techniques of auto calibration such as measuring the noise in situ and cycling a bank of switches for the tune point.

Discussion

What is really happening?

Achieving null was so fine that signal levels were negligibly changed. The results show that the flicker noise behaved as if it always running open loop irrespective of closed loop gain. This suggests that nothing is happening at all to the noise. It is how the noise is being treated.

Applying Occam's razor.

The most straight forward explanation of up-conversion noise is VCO modulation. This usually requires a non-linear capacitor. By inspection of the topology, it is obvious that there are several non-linear capacitors, all of which have values of a significant percentage to the tank capacitance. These are C_{dg} , C_{gs} and C_{ds} of the mosfets. To some extent, as one half of the oscillator increases its gate capacitance, the other reduces its gate capacitance. However, there is not complete cancellation. In general, any noise appearing across the mosfet capacitances will still modulate the frequency of the oscillator.

Despite the fact that HL_LTV theory is incorrect, there is some merit in the stand alone idea that a zero value for the integral of a correct non-linear ISF of a correct ISF theory results in zero up-converted noise. The key point being that it is the integral being zero, not that the waveforms should be symmetrical. They are not symmetrical in the above topology, however, it is quite possible to have a triangle positive cancelling a

rectangular negative if they have equal areas. It is suggested here that the correct choice of RS here modifies the real ISF such that its integral is indeed zero.

Observations

It is noted from web searches that considerable effort has been undertaken in order to eliminate 1/f noise in differential oscillators. Many of these oscillators use bias current sources, and it is the 1/f noise of these current sources that are typically being dealt with. It is noted here that the simplest way to deal with this difficult task, is simply, never to use them. This would leave only the differential pair noise to deal with.

It is noted that 1mm by 1mm, 10k analog sized transistors, in 0.18u BiCMOS process can be had for only 10 cents. The topology shown here has quite a stable bias current, being determined by the power supply voltage, source resistor and V_t/K variations. Of course, if the oscillator was running on the same supply as an audio amplifier, even a 1 ma variable drop in a 1 ohm supply lead could lead to an intolerable 1 mv low frequency modulation of the oscillator. The solution is simply to use a mere 50 of those transistors to form a low noise dedicated bandgap regulator for the oscillator. This has the advantage that very large Mosfets may be used to reduce its 1/f noise. Such large mosfets would not be so useable as a current source for a high frequency oscillator. What matters, is the best way to achieve a system ASIC design, not the best way to design one particular block in the system ASIC.

Conclusions

The argument that there is some kind of “nulling of the flicker noise” or reduction of actual noise due to any capacitor or reduced effect of low frequency noise is not supportable. Graphs with and without the conventional low frequency gain reducing capacitor overlaid each other. The capacitor was not necessary in order to achieve perfect elimination of flicker noise for any circuit configuration.

It has been shown that complete nulling of 1/f noise may be achieved by simple choosing the correct mosfet sizes and source tail resistor!

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